ABSTRACT

An on-chip circuit for defect testing with the ability to maintain a substrate voltage at a level more positive or more negative than a normal negative operating voltage level of the substrate. This is accomplished with a chain of MOSFETs that are configured to operate as a chain of resistive elements or diodes wherein each element in the chain may drop a portion of a supply voltage coupled to a first end the chain. The substrate is coupled to a second end of the chain. The substrate voltage level is essentially equivalent to the supply voltage level less the voltage drops across the elements in the diode chain. A charge pump maintains the substrate voltage level set by the chain. Performing chip testing with the substrate voltage level more negative than the normal negative voltage level facilitates detection of devices that will tend to fail only at cold temperatures. Performing chip testing with the substrate voltage level more positive than the normal negative voltage level facilitates detection of other margin failures and ion contamination.